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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,670	07/28/2003	Ted Humphrey		4437

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EXAMINER	
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ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,670	HUMPHREY, TED	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) 3, 5, 14-19, 21 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1, 2, 4, 6-13, 20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election of Species III in the reply filed on 11-29-2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1, and 4-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims like claim 1 recite circuits with "new topologies" which makes the scope of the claims indefinite for it cannot be determined what these "new topologies" are or will be. Note that claims 4-21 are included because of the dependency of these claims either directly or indirectly on claim 1 and these claims do not appear to define what structure applicant meant by this terminology. Note that many of these claims 4-21 are non-elected and will be indicated on the PTOL-326 as such.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Smith et al. 5,469,104 (Smith).

Figures 4C and 4D and the relevant text of Smith discloses an analog electronic amplifier device having a four terminal device composed of bipolar transistors 52 and 54 of like conductivity. The "terminal 1" i.e. the first terminal is formed by the node between the base of 52 and the collector of transistor 54 and does accept a current of predetermined direction from current source 58 as is clearly

illustrated by Smith. "Terminal 2" i.e. the second terminal is formed by the node connected to the emitter of transistor 54. This terminal receives and input signal V_{r2}. Note that in the elected species with applicant states that claims like claim 1 are directed that the input signal is ground. Also note that terminal 2 of Figure 10 that makes up at least in part the Figure 13 species shows terminal 2 as the terminal directly connected to the emitter. As the Smith reference shows the same structure as claimed and disclosed this terminal 2 of Smith must be receptive to an input signal and is fully capable of being receptive to an input signal. "Terminal 3", i.e. the third terminal is formed by the collector of the transistor 52 which is the same as that of applicant's discloses and claimed invention where the collector of transistor Q3 forms the third terminal. Smith clearly shows current I_a flowing from transistor 52 and thus terminal 3 of Smith "causes a current to flow". "Terminal 4" i.e. the fourth terminal of Smith is formed by the node between the emitter of transistor 52 and the base of transistor 54 which is the same as the terminal 4 of applicant wherein this terminal 4 is formed by the node between the emitter of transistor Q_3 and the base of transistor Q_1. Because the Smith reference has all the claimed structure the Smith reference is fully capable of performing the recited function. Transistor 54 forms the first transistor in Smith and transistor 52 forms the second transistor in Smith. Thus "said terminal 1 is the connection of the base of said second transistor and the collector of said first transistor; said terminal 2 is the emitter of said first transistor; said terminal 3 is the collector of said second transistor; said terminal 4 is the connection of the base of said first transistor and the emitter of said second transistor" is clearly met by Smith. Because the Smith reference has all the claimed structure that applicant attributes the sensing device of Figure 13 to mean of the instant application, Smith is seen as also having the "sensing device". In other words applicant states that claim 4 is directed toward Figure 13 and Smith showing the structure of Figure 13 that includes the sensing device as meant by applicant.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Darlington 2,663,806 (Darlington).

Figure 7 of Darlington discloses the same exact arrangement like that set forth in Figure 7 of the disclosed invention. As set forth by the claims and Figure 7 of the specification the transistor device has four terminals labeled 1-4. The first terminal "1" as claimed and disclosed is terminal 18' in Darlington. The second terminal "2" as claimed and disclosed is terminal "b" in Darlington. The third terminal "3" as claimed and disclosed is terminal "18" in Darlington and the fourth terminal "4" as claimed and discloses is the terminal "e" in Darlington. Claims like claim 1 recites that the first terminal "accepts a current of predetermined direction". This is a very broad limitation in that no source is recited as being connected to this terminal. The terminal being conductive in nature is the means by which the terminal accepts a current of a predetermined direction. The terminals of Darlington are conductive in nature which provide the means such that terminal 1 accepts a current of predetermined direction, terminal 1 is receptive to any signal applied thereto. Because the claims do not recite any source connected to this terminal 1, the Darlington reference has all the claimed structure. Thus Darlington is fully capable of performing the recited function of the first terminal being capable of accepting a current of a predetermined direction. Note that a predetermined direction is a broad limitation and could include a bi-directional signal as this is a signal of a predetermined direction. Likewise, the second terminal is receptive to an input signal. No input signal source is claimed and the Darlington has all the claimed structure. In fact the Darlington reference intends to connect the second terminal to some source as it is to be an art recognized equivalent to a single transistor. Just like applicant's invention the connection of these two transistors in Darlington is what make the third terminal to cause current to flow. In fact column 6, around line 59 recites that source may be connected to this terminal which clearly results in this terminal accepting a current of a predetermined direction. Just like applicant's invention the connection of these two transistors in Darlington is the "means to concurrently produce an output voltage and current in response to the voltage and current at said terminal 2 and to sense said voltage and current at said terminal 4 and to adjust said voltage and current at said terminal 2 and said current at said terminal 3." Column 1 of Darlington clearly relates to the utilization of the circuit as a replacement for a transistor in larger circuits. Thus the device of Darlington is fully capable of performing the recited function of being usable "can be used" in other transistor based systems such as amplifiers, etc. However, Darlington is silent on naming the specific circuits to which the claimed invention of the instant application can be used i.e. circuits like "amplifiers", cascading devices",...etc. Alternatively, since these circuits, i.e. amplifiers are commonly composed of transistors, Darlington teaches that his circuit is an art recognized equivalent to a single transistor and

Darlington is a component of a larger system. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the circuit of Darlington in any transistor based system such as an amplifier, etc. because, as the Darlington reference is silent on the exact system to use the component one of ordinary skill in the art would have been motivated to use the component in any art recognized system that employs transistors such as amplifiers, cascading device, buffers, regulators and "digital circuits with new topologies". Note that the two bipolars of Darlington are for like conductivity (See Figure 7 of Darlington).

Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maschmann et al. 5,465,074 (Maschmann) in view of Smith et al. 5,469,104 (Smith) as evidenced by Darlington 2,663,806 (Darlington).

Maschmann discloses the basic three stage "symmetrical" amplifier as claimed. Note that Q1 would form in part a first stage, Q3 forms in part the second and Q5 in combination with Q11 forms in part the third stage. Likewise Q2, Q4 and Q6 in combination with Q12 forms the three stage of the symmetrical other leg of the amplifier and are of an opposite polarity compared to the first "leg" of the arrangement. "IN" is a composite input wherein the inputs of the first stages are connected together. "OUT" is clearly a composite output. Note that applicant calls the third stage the second stage and the second stage the "buffer". One difference between Maschmann and the claimed invention is in the selection of the transistors arrangements like Q3 and Q4 to be composed of a "four terminal device" i.e. two transistors connected together with an input source. Note that reference point of the second stage is coupled to ground. The claims like claim 9 recites the use of the reference point as a "non-inverting input". Because this is the same structure as presented by applicant this terminal is fully capable of functioning as a non-inverting terminal. As noted in the previous office action Figures 13, 14 and 19 are not considered to be patentable distinct over one another. They are directed to the same species. Applicant has not argued this. Note that one can call the arrangement of Maschmann a buffer for this is an amplifier. However, alternatively the selection of the overall gain is merely a result effective variable wherein this selection is of the optimum or workable range. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the overall gain to be unit as this involves but routine skill in the art.

Smith discloses such an arrangement in Figures 4c and 4d as noted above in the rejection of claims 1, 2, 4 and 20 as being anticipated by Smith. Applicant is referenced to this rejection above concerning the details of how this structure meets the claimed four terminal device. Smith is silent on

calling this four terminal device an equivalent to a single transistor arrangement, however, such is the case and Figure 7 of Darlington provides the evidence that the four terminal structure arrangement of Smith is the art recognized equivalent to a single transistor. Note that like above the because the Smith arrangement has the same four terminal arrangement and associated circuitry the arrangement of Smith is seen as providing for the recited structure.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the four terminal device arrangement of Smith for the second stage amplifier arrangement of Maschmann given the art recognized equivalence of these structures as evidenced by Darlington.

Since the structure made obvious above has the same structure as claimed the recited functions of this combination is an obvious consequence of the structure made obvious above. Also note that the second stage would have to be a npn stage in order for the device to function properly.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maschmann et al. 5,465,074 (Maschmann) in view of Smith et al. 5,469,104 (Smith) as evidenced by Darlington 2,663,806 (Darlington) as applied to claims 6-9 and 11 above, and further in view of Servaes 6,204,730 (Servaes).

Maschmann and Smith as evidenced by Darlington 2,663,806 (Darlington) above and the following. Claim 10 is directed toward the use of an additional stage on the output of the amplifier. The number of stages provides for an desired overall gain and an overall ability to drive a load. For example the addition of a buffer does not change the gain but allow the device connected thereto to drive multiple loads.

Servaes discloses a power amplifier arrangement to drive a load 10.

Given that it is well known to cascade amplifier arrangements it would have been obvious to one of ordinary skill in the art to have cascaded the arrangement of Maschmann and Smith and Darlington made obvious above with that of Servaes so as to select the proper gain and provide the additional drive capabilities as is known in the art.

In addition to that above, Figure 1 of Servaes discloses the basic output circuitry of claims 10. This includes two common collector amplifiers 13 and 14 in cascade in a symmetrical arrangement with two common collector amplifiers 21 and 22 of opposite polarity. Like above. Note that one can call the arrangement of Servaes a buffer for this is an amplifier. However, alternatively the selection of the overall gain is merely a result effective variable wherein this selection is of the optimum or workable range. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the overall gain to be unit as this involves but routine skill in the art. One difference

between Servaes and the claimed invention is in the selection of the transistors arrangements like 13 and 21 to be composed of a "four terminal device" i.e. two transistors connected together with an input source.

Smith discloses such an arrangement in Figures 4c and 4d as noted above in the rejection of claims 1, 2, 4 and 20 as being anticipated by Smith. Applicant is referenced to this rejection above concerning the details of how this structure meets the claimed four terminal device. Smith is silent on calling this four terminal device an equivalent to a single transistor arrangement, however, such is the case and Figure 7 of Darlington provides the evidence that the four terminal structure arrangement of Smith is the art recognized equivalent to a single transistor. Note that like above the because the Smith arrangement has the same four terminal arrangement and associated circuitry the arrangement of Smith is seen as providing for the recited structure.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the four terminal device arrangement of Smith for the 13 and 21stage amplifier arrangements of Servaes given the art recognized equivalence of these structures as evidenced by Darlington.

Since the structure made obvious above has the same structure as claimed the recited functions of this combination is an obvious consequence of the structure made obvious above.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Servaes 6,204,730 (Servaes) in view of Smith et al. 5,469,104 (Smith) as evidenced by Darlington 2,663,806 (Darlington).

Figure 1 of Servaes discloses the basic circuitry of claims 11 and 12. This includes two common collector amplifiers 13 and 14 in cascade in a symmetrical arrangement with two common collector amplifiers 21 and 22 of opposite polarity. Like above. Note that one can call the arrangement of Servaes a buffer for this is an amplifier. However, alternatively the selection of the overall gain is merely a result effective variable wherein this selection is of the optimum or workable range. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the overall gain to be unit as this involves but routine skill in the art. One difference between Servaes and the claimed invention is in the selection of the transistors arrangements like 13 and 21 to be composed of a "four terminal device" i.e. two transistors connected together with an input source.

Smith discloses such an arrangement in Figures 4c and 4d as noted above in the rejection of claims 1, 2, 4 and 20 as being anticipated by Smith. Applicant is referenced to this rejection above

concerning the details of how this structure meets the claimed four terminal device. Smith is silent on calling this four terminal device an equivalent to a single transistor arrangement, however, such is the case and Figure 7 of Darlington provides the evidence that the four terminal structure arrangement of Smith is the art recognized equivalent to a single transistor. Note that like above the because the Smith arrangement has the same four terminal arrangement and associated circuitry the arrangement of Smith is seen as providing for the recited structure.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the four terminal device arrangement of Smith for the 13 and 21stage amplifier arrangements of Servaes given the art recognized equivalence of these structures as evidenced by Darlington.

Since the structure made obvious above has the same structure as claimed the recited functions of this combination is an obvious consequence of the structure made obvious above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
February 14, 2005

Michael B Shingleton
Primary Examiner
GROUP ART UNIT 2817